WE CLAIM:

1. A method for manufacturing a semiconductor integrated circuit device comprising the steps of:

(a) forming an isolation trench in an isolation region of a semiconductor substrate;

(b) filling said isolation trench up to predetermined middle position in its depth direction with a first insulating film deposited by a coating method;

(c) filling a remaining depth portion of said isolation trench into which said first insulating film is filled with a second insulating film;

(d) forming a plurality of patterns on said semiconductor substrate after said step (c);

(e) filling a trench forming between said plurality of patterns up to predetermined middle position in a trench depth direction with a third insulating film deposited by a coating method; and

(f) filling a remaining portion of said trench into which said third insulating film is filled with a fourth insulating film, wherein said fourth insulation film is more difficult to etch than said third insulating film.

2. A method for manufacturing a semiconductor integrated circuit device comprising the steps of:

(a) forming isolation trenches in isolation regions with relatively different planar dimensions on a semiconductor substrate;

(b) filling said isolation trenches up to predetermined middle position in their depth direction with a first insulating film deposited by a coating method; and

(c) filling a remaining depth portion of said isolation trenches into which said first insulating film is filled with a second insulating film; and

forming dummy patterns in a relatively large isolation region of isolation regions with relatively different planar dimensions before said first insulating film is deposited.

3. A method for manufacturing a semiconductor integrated circuit device comprising the step of:

(a) forming an isolation trench in an isolation region of a semiconductor substrate;

(b) filling said isolation trench up to predetermined middle position in its depth direction with a first insulating film deposited by a coating method;

(c) filling a remaining depth portion of said isolation trench into which said first insulating film is filled with a second insulating film;

(d) forming a plurality of patterns on said semiconductor substrate after said step (c);

(e) filling a trench forming between said plurality of patterns up to predetermined middle position in a trench depth direction with a third insulating film deposited by a coating method; and

(f) filling a remaining portion of said trench into which said third insulating film, is filled with a fourth insulating film being more difficult to etch than said third insulating film; and

forming dummy patterns in a relatively large isolation region of isolation regions with relatively different planar dimensions when said isolation trenches are formed.

4. A method for manufacturing a semiconductor integrated circuit device comprising the steps of:

(a) forming isolation trenches in isolation regions with relatively different planar dimensions on a semiconductor substrate;

(b) filling said isolation trenches up to predetermined middle position in their depth direction with a first insulating film deposited by a coating method;

(c) filling a remaining depth portion of said isolation trenches into which said first insulating film is filled with a second insulating film; and

forming dummy patterns between said isolation trenches in a relatively large isolation region of isolation regions with relatively different planar dimensions when said isolation trenches are formed such that a planer dimension difference and depth dimension difference of said isolation trenches in said isolation regions with relatively different

planar dimensions, respectively, are small.

5. A method for manufacturing a semiconductor integrated circuit device comprising the steps of:

a) forming isolation trenches in isolation regions with relatively different planar dimensions on a semiconductor substrate;

b) filling said isolation trenches up to predetermined middle position in their depth direction with a first insulating film deposited by a coating method;

c) filling a remaining depth portion of said isolation trenches into which said first insulating film is filled with a second insulating film; and

forming dummy patterns between said isolation trenches in a relatively large

isolation region of isolation regions with relatively different planar dimensions when said isolation trenches are formed such that a planer dimension and depth dimension of said isolation trenches in said isolation regions with relatively different planar dimensions, respectively are equal in design.

6. A method for manufacturing a semiconductor integrated circuit device according to claim 2, wherein said first insulating film is filled into said isolation trenches at said (b) step such that a thickness of said first insulating film is uniform within isolation trenches formed in said isolation regions with relatively different planar dimensions, respectively.

7. A method for manufacturing a semiconductor integrated circuit device according to claim 1 wherein said step (b) comprises the steps of depositing said first insulating film on a main surface of said semiconductor substrate by a coating method such that the deposited first insulating film has a planarized surface, and then etching back said first insulating film.

8. A method for manufacturing a semiconductor integrated circuit device according to claim 1 wherein, after said first insulating film is filled into said isolation trench, thermal processing is performed on said first insulating film.

9. A method for manufacturing a semiconductor integrated circuit device according to claim 2, further comprising the steps of:

(d) forming a plurality of patterns on said semiconductor substrate after said

step (c);

(e) filling a trench formed between said plurality of patterns up to predetermined middle position in a trench depth direction with a third insulating film deposited by a coating method; and

(f) filling a remaining portion of said trench into which said third insulating film, is filled with a fourth insulating film.

10. A method for manufacturing a semiconductor integrated circuit device comprising the steps of:

(a) forming a plurality of patterns, which are adjacent to each other, on a semiconductor substrate;

(b) filling a trench formed between said plurality of patterns, which are adjacent to each other, up to predetermined middle position in its depth direction with a first insulating film deposited by a coating method; and

(c) filling a remaining depth portion of said trench into which said first insulating film is filled with a second insulating film.

11. A method for manufacturing a semiconductor integrated circuit device according to claim 10 wherein said plurality of patterns include a MISFET gate electrode and a dummy gate electrode.

12. A method for manufacturing a semiconductor integrated circuit device according to claim 11 wherein said second insulating film is deposited by a chemical vapor deposition method.

13. A method for manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a plurality of word lines adjacent to each other on a semiconductor substrate, which form a gate electrode of a field effect transistor for memory cell selection;

(b) depositing an insulating film on said semiconductor substrate so as to cover a surface of said plurality of word lines;

(c) filling a trench formed between said plurality of word lines up to predetermined middle position in its depth direction with a first insulating film deposited by a coating method;

(d) filling a remaining depth portion of said trench into which said first insulating film is filled trench into which said first insulating with a second insulating film deposited by a chemical vapor deposition method;

(e) punching a hole on said insulating film and said first and second insulating films between said adjacent plurality of word lines so as to reach to a pair of semiconductor regions of said field effect transistor for memory cell selection;

(f) forming a bit line electrically connected to one semiconductor region of said pair of semiconductor regions of said field effect transistor for said memory cell selection through said hole; and

(g) forming an information storage capacitor element electrically connected to the other semiconductor region of said pair of semiconductor regions of said field effect transistor for memory cell selection through said hole,

the step of punching a hole on said insulating film and said first and second insulating films comprising the steps of:

performing etching processing on said insulating film and said first and second insulating films by having a relatively large etching selection ratio between said insulating film and said first and second insulating films and under condition that said first and second insulating films are easier to be etched and removed than said insulating film, and then performing etching processing on said insulating film and said first and second insulating films under condition that said insulating film is easier to be etched and removed than said first and second insulating films.

14. A method for manufacturing a semiconductor integrated circuit device according to claim 10, the step of filling said first insulating film comprising the step of depositing said first insulating film on a main surface of said semiconductor substrate by a coating method and then etching back said first insulating film so as to leave it within said trench.

15. A method for manufacturing a semiconductor integrated circuit device according to claim 10, wherein thermal processing is performed on said first insulating film after said first insulating film is filled into said trench.

16. A method for manufacturing a semiconductor integrated circuit device according to claim 1, wherein said first insulating film has liquidity with a 100 mPa•s or lower viscosity coefficient at a temperature of 25 °C.

17. A method for manufacturing a semiconductor integrated circuit device according to claim 1, wherein said second insulating film is formed by a chemical vapor deposition method using mixture gas of tetraethoxysilane and ozone or by a chemical vapor deposition method for decomposing mixture gas of monosilane and oxygen with high density plasma.

18. A semiconductor integrated circuit device, wherein an isolation portion formed in an isolation region of a semiconductor substrate includes an isolation trench dug in said isolation regions with relatively different planer dimensions, respectively in a thickness direction of said semiconductor substrate, a first insulating film formed by a coating method such that said isolation trench is filled up to predetermined middle position of its depth direction, and a second insulating film formed by a chemical vapor deposition method so as to fill a remaining depth portion of said isolation trench into which said first insulating film is filled.

19. A semiconductor integrated circuit device comprising isolation regions with relatively different planar dimensions arranged on a main surface of a semiconductor substrate, an isolation trench dug in said isolation regions with relatively different planar dimensions, respectively ma thickness direction of said semiconductor substrate, a first insulating film formed by a coating method such that said isolation

trench is filled up to predetermined middle position of its depth direction, and a second insulating film formed by a chemical vapor deposition method so as to fill a remaining depth portion of said isolation trench into which said first insulating film is filled, wherein a dummy pattern is provided between said isolation trenches formed in an isolation region with a relatively large planar dimension of said isolation regions with relatively different planar dimensions.

20. A semiconductor integrated circuit device according to claim 19, wherein a thickness of said first insulating film is uniform within isolation trenches formed in said isolation regions with relatively different planar dimensions, respectively.

21. A semiconductor integrated circuit device comprising a plurality of patterns adjacent to each other formed on a semiconductor substrate, a first insulating film deposited by a coating method such that a trench formed between said plurality of patterns adjacent to each other is filled up to predetermined middle position in its depth direction, and a second insulating film deposited by a chemical vapor deposition method so as to fill a remaining depth portion of said trench into which said first insulating film is filled.

22. A semiconductor integrated circuit device, comprising:

a plurality of field effect transistors for memory cell selection formed on a semiconductor substrate;

a plurality of word lines, which are wires forming a gate electrode of said field effect transistor for memory cell selection, formed adjacent to each other on a main

surface of said semiconductor substrate;

an insulating film on said semiconductor substrate so as to cover a surface of said plurality of word lines;

a first insulating film deposited by a coating method so as to fill a trench formed between said plurality of word lines up to predetermined middle position in its depth direction;

a second insulating film deposited by a chemical vapor deposition method so as to fill a remaining depth portion of said trench into which said first insulating film is filled;

a hole arranged two-dimensionally between said adjacent plurality of word lines and formed on said insulating film and said first and second insulating films so as to expose a pair of semiconductor regions of said field effect transistor for memory cell selection;

a bit line electrically connected to one semiconductor region of said pair of semiconductor regions of said field effect transistor for said memory cell selection through said hole; and

an information storage capacitor element electrically connected to the other semiconductor region of said pair of semiconductor regions of said field effect transistor for memory cell selection through said hole.

23. A method for manufacturing a semiconductor integrated circuit device according to claim 1, wherein said plurality of patterns include a MISFET gate electrode.

24. A method for manufacturing a semiconductor integrated circuit device according to claim 1 wherein said second insulating film is deposited by a chemical vapor deposition method.

25. A semiconductor integrated circuit device according to claim 21 wherein said plurality of patterns include a MISFET gate electrode and a dummy gate electrode.

26. A semiconductor integrated circuit device according to claim 25 wherein said second insulating film is deposited by a chemical vapor deposition method.

27. A method for manufacturing a semiconductor integrated circuit device according to claim 10, wherein said plurality of patterns are dummy patterns provided in an isolation trench in an isolation region.

28. A semiconductor integrated circuit device according to claim 21, wherein said plurality of patterns are dummy patterns provided in an isolation trench in an isolation region.

29. A method for manufacturing a semiconductor integrated circuit device according to claim 1, wherein said first insulating film is filled into said isolation trenches at said (b) step such that a thickness of said first insulating film is uniform within isolation trenches formed in said isolation regions with relatively different planar dimensions, respectively.

30. A method for manufacturing a semiconductor integrated circuit device according to claim 3, wherein said first insulating film is filled into said isolation trenches at said (b) step such that a thickness of said first insulating film is uniform within isolation trenches formed in said isolation regions with relatively different planar dimensions, respectively.

31. A method for manufacturing a semiconductor integrated circuit device according to claim 4, wherein said first insulating film is filled into said isolation trenches at said (b) step such that a thickness of said first insulating film is uniform within isolation trenches formed in said isolation regions with relatively different planar dimensions, respectively.

32. A method for manufacturing a semiconductor integrated circuit device according to claim 1, further comprising the steps of:

(d) forming a plurality of patterns on said semiconductor substrate after said step (c), wherein said plurality of patterns include a MISFET gate electrode and a dummy gate electrode;

(e) filling a trench formed between said plurality of patterns up to a middle position in a trench depth direction with a third insulating film deposited by a coating method; and

(f) filling a remaining portion of said trench into which said third insulating film is filled, with a fourth insulating film.

33. A method for manufacturing a semiconductor integrated circuit device according to claim 3, further comprising the steps of:

(d) forming a plurality of patterns on said semiconductor substrate after said step (c), wherein said plurality of patterns include a MISFET gate electrode and a dummy gate electrode;

(e) filling a trench formed between said plurality of patterns up to a middle position in a trench depth direction with a third insulating film deposited by a coating method; and

(f) filling a remaining portion of said trench into which said third insulating film is filled, with a fourth insulating film.

34. A method for manufacturing a semiconductor integrated circuit device according to claim 4, further comprising the steps of:

(d) forming a plurality of patterns on said semiconductor substrate after said step (c), wherein said plurality of patterns include a MISFET gate electrode and a dummy gate electrode;

(e) filling a trench formed between said plurality of patterns up to a middle position in a trench depth direction with a third insulating film deposited by a coating method; and

(f) filling a remaining portion of said trench into which said third insulating film is filled, with a fourth insulating film.

35. A method for manufacturing a semiconductor integrated circuit device comprising the step of:

(a) forming an isolation trench in an isolation region of a semiconductor substrate

(b) filling said isolation trench up to predetermined middle position in its depth direction with a first insulating film deposited by a coating method;

(c) filling a remaining depth portion of said isolation trench into which said first insulating film is filled with a second insulating film;

(d) forming a plurality of patterns on said semiconductor substrate after said step (c);

(e) filling a trench forming between said plurality of patterns up to predetermined middle position in a trench depth direction with a third insulating film deposited by a coating method;

(f) filling a remaining portion of said trench into which said third insulating film is filled with a fourth insulating film being more difficult to etch than said third insulating film; and

(g) forming a hole on said semiconductor substrate by etching said fourth insulating film and said third insulating film.

(h) filling a conductive layer into said hole;

(i) after said step (h), forming a fifth insulating film on said fourth insulating film and said conductive layer; and

(j) forming a hole exposing said conductive layer in said fifth insulating film by etching said fifth insulating film.

36. A method for manufacturing a semiconductor integrated circuit device according to claim 1, further comprising the steps of:

(g) forming a hole on said semiconductor substrate by etching said fourth insulating film and said third insulating film;

(h) depositing a conductive layer into said hole;

(i) forming a fifth insulating film on said fourth insulating film and said conductive layer; and

(j) forming a hole connected said conductive layer by etching said fifth insulating film.

37. A method for manufacturing a semiconductor integrated circuit device according to claim 1, wherein said step (e) comprises the steps of depositing said third insulating film on main surface of said semiconductor substrate by a coating method such that said deposited third insulating film has a planized surface and then etching back said first insulating film.

38. A method for manufacturing a semiconductor integrated circuit device according to claim 1, wherein after said third insulating film is filled into said trench, thermal processing is performed on said third insulating film.

39. A method for manufacturing a semiconductor integrated circuit device according to claim 1, wherein said third insulating film has liquidity with a 100 mPa•s or lower viscosity coefficient at a temperature of 25°C.

40. A method for manufacturing a semiconductor integrated circuit device according to claim 1, wherein said fourth insulating film is deposited by a chemical vapor deposition method.

41. A method for manufacturing a semiconductor integrated circuit device according to claim 3, further comprising the steps of:

(g) forming a hole on said semiconductor substrate by etching said fourth insulating film and said third insulating film;

(h) depositing a conductive layer into said hole;

(i) forming a fifth insulating film on said fourth insulating film and said conductive layer; and

(j) forming a hole connected said conductive layer by etching said fifth insulating film.